CLAIMS

What is claimed is:

1. A method for electrically connecting semiconductor component substrates, comprising:

providing a first semiconductor component substrate having at least one interconnect element on a surface thereof;

disposing a dielectric element having at least one cavity therein on the surface of the first semiconductor component substrate, with the at least one cavity located over the at least one interconnect element;

providing a second semiconductor component substrate having at least another interconnect element on a surface thereof;

securing the second semiconductor component substrate to the first semiconductor component substrate with the dielectric element interposed therebetween and the at least another interconnect element of the second semiconductor component substrate aligned with the at least one cavity to form at least one interconnect void; and

injecting a flowable conductive material into the at least one interconnect void through one of the first and second semiconductor component substrates to form at least one conductive interconnect structure between the at least one and the at least another interconnect elements.

2. The method according to claim 1, wherein providing a first semiconductor component substrate having at least one interconnect element on a surface thereof comprises providing a semiconductor die having at least one bond pad on a surface thereof.

3. The method according to claim 1, wherein providing a second semiconductor component substrate having at least another interconnect element on a surface thereof comprises providing a carrier substrate having at least one terminal pad on a surface thereof.

4. The method according to claim 1, wherein disposing a dielectric element on the surface of the first semiconductor component substrate comprises disposing one of a flowable dielectric material and a preformed dielectric element on the surface of the first semiconductor component substrate.

5. The method according to claim 1, further comprising selecting the flowable conductive material to comprise one of a conductive polymer, a conductor-filled polymer, a conductive paste, and a molten solder.

6. The method according to claim 1, wherein injecting a flowable conductive material into the at least one interconnect void through one of the first and second semiconductor component substrates comprises inserting an injection needle through one of the first and second semiconductor component substrates and into the at least one interconnect void.

7. The method according to claim 6, wherein inserting an injection needle through one of the first and second semiconductor component substrates comprises perforating the one of the first and second semiconductor component substrates with the injection needle.

8. The method according to claim 7, further including forming at least one vent aperture to one side of the injection needle concurrently with the perforation of the one of the first and second semiconductor component substrates.

9. The method according to claim 7, wherein perforating the one of the first and second semiconductor component substrates comprises contacting an interconnect element associated with the at least one interconnect void with the injection needle.

10. The method according to claim 9, wherein contacting the interconnect element associated with the at least one interconnect void comprises perforating the interconnect element with the injection needle.

11. The method according to claim 7, further comprising contacting the dielectric element with the injection needle.

12. The method according to claim 11, wherein contacting the dielectric element with the injection needle comprises perforating the dielectric element with the injection needle.

13. The method according to claim 6, further comprising orienting the injection needle substantially perpendicular to a plane of the one of the first and second semiconductor component substrates through which the injection needle is inserted.

14. The method according to claim 6, further comprising orienting the injection needle in a nonperpendicular relationship to a plane of the one of the first and second semiconductor component substrates through which the injection needle is inserted.

15. The method according to claim 6, further comprising disposing a tip of the injection needle adjacent to a side of the at least one interconnect void.

16. The method according to claim 6, further comprising withdrawing the injection needle from the at least one interconnect void during the injecting of the flowable conductive material thereinto.

17. The method according to claim 7, further including sealing an open perforation formed by insertion of the injection needle after withdrawal thereof with a dielectric sealing material.

18. The method according to claim 17, wherein sealing comprises occluding the open perforation.

19. The method according to claim 18, wherein occluding the open perforation comprises disposing a layer of the dielectric sealing material over an exposed surface of the one of the first and second semiconductor component substrates.

20. The method according to claim 6, wherein inserting an injection needle through one of the first and second semiconductor component substrates comprises inserting the injection needle through an injection port extending to the at least one interconnect void.

21. The method according to claim 20, further comprising forming the injection port through the one of the first and second semiconductor component substrates.

22. The method according to claim 21, further comprising forming the injection port through an interconnect element.

23. The method according to claim 21, further comprising forming the injection port adjacent an interconnect element.

24. The method according to claim 21, further including forming a vent port through one of the first and second semiconductor component substrates and extending to the at least one interconnect void.

25. The method according to claim 24, further including sealing the vent port with a dielectric sealing material after withdrawal of the injection needle.

26. The method according to claim 25, wherein sealing comprises occluding the vent port.

27. The method according to claim 26, wherein occluding the vent port comprises disposing a layer of the dielectric sealing material over an exposed surface of the one of the first and second semiconductor component substrates.

28. The method according to claim 20, further including sealing the injection port with a dielectric sealing material after withdrawal of the injection needle.

29. The method according to claim 28, wherein sealing comprises occluding the injection port.

30. The method according to claim 29, wherein occluding the injection port comprises disposing a layer of the dielectric sealing material over an exposed surface of the one of the first and second semiconductor component substrates.

31. The method according to claim 1, wherein injecting a flowable conductive material into the at least one interconnect void comprises injecting a molten solder into the at least one interconnect void.

32. The method according to claim 31, wherein the flowable conductive material comprises a molten solder and further comprising fluxing the interconnect elements prior to injecting the molten solder.

33. The method according to claim 1, wherein injecting a flowable conductive material into the at least one interconnect void to form at least one conductive interconnect structure comprises substantially filling a volume of the at least one interconnect void with the flowable conductive material.

34. The method according to claim 1, further comprising selecting one of the first and second semiconductor component substrates to comprise a semiconductor die and selecting another of the first and second semiconductor component substrates to comprise a carrier substrate.

35. The method according to claim 1, further comprising selecting a thickness for the dielectric element to at least in part determine a volume of the at least one interconnect void.

36. The method according to claim 1, wherein the at least one interconnect element comprises a plurality of interconnect elements, the at least another interconnect element comprises a like plurality of another interconnect elements, and the at least one interconnect void comprises a like plurality of interconnect voids therebetween.

37. The method according to claim 36, further comprising simultaneously inserting a plurality of injection needles into a like plurality of interconnect voids.

38. The method according to claim 37, further comprising simultaneously injecting the flowable conductive material into the like plurality of interconnect voids.

39. A method for electrically connecting semiconductor component substrates, comprising:

providing a first semiconductor component substrate having at least one interconnect element on a surface thereof;

disposing a dielectric element having at least one cavity therein on the surface of the first semiconductor component substrate, with the at least one cavity located over the at least one interconnect element;

disposing a mass of conductive material in the at least one cavity;

providing a second semiconductor component substrate having at least another interconnect element on a surface thereof;

securing the second semiconductor component substrate to the first semiconductor component substrate with the dielectric element interposed therebetween and the at least another interconnect element of the second semiconductor component substrate aligned with the at least one cavity to form at least one interconnect void; and

altering the mass of conductive material to a flowable state to form at least one conductive interconnect structure within the at least one interconnect void extending between the at least one interconnect element and the at least another interconnect element.

40. The method according to claim 39, further comprising selecting the mass of conductive material from solder, a solder paste, conductive thermoplastic resin and conductor-filled thermoplastic resin.

41. The method according to claim 39, further comprising heating the mass of conductive material to alter it to the flowable state.

42. The method according to claim 41, further comprising heating the mass of conductive material using ultrasonic energy.

43. The method according to claim 39, further comprising allowing the conductive material in the flowable state to transform to a solid state in contact with the at least one interconnect element and the at least another interconnect element.

44. The method according to claim 39, further comprising selecting a volume for the mass of conductive material to substantially fill the at least one interconnect void.

45. The method according to claim 39, wherein providing a first semiconductor component substrate having at least one interconnect element on a surface thereof comprises providing a semiconductor die having at least one bond pad on a surface thereof.

46. The method according to claim 39, wherein providing a second semiconductor component substrate having at least another interconnect element on a surface thereof comprises providing a carrier substrate having at least one terminal pad on a surface thereof.

47. The method according to claim 39, wherein disposing a dielectric element on the surface of the first semiconductor component substrate comprises disposing one of a flowable dielectric material and a preformed dielectric element on the surface of the first semiconductor component substrate.

48. The method according to claim 39, further comprising selecting one of the first and second semiconductor component substrates to comprise a semiconductor die and selecting another of the first and second semiconductor component substrates to comprise a carrier substrate.

49. The method according to claim 39, further comprising selecting a thickness for the dielectric element to at least in part determine a volume of the at least one interconnect void.

50. The method according to claim 39, wherein the at least one interconnect element comprises a plurality of interconnect elements, the at least another interconnect element comprises a like plurality of another interconnect elements, and the at least one interconnect void comprises a like plurality of interconnect voids therebetween.

51. The method of claim 50, further comprising simultaneously heating preformed masses of conductive material in the like plurality of interconnect voids.

52. A semiconductor component assembly, comprising:

a first semiconductor component substrate including a plurality of interconnect elements on a surface thereof;

a second semiconductor component substrate including another, like plurality of interconnect elements on a surface thereof arranged in alignment with the plurality of interconnect elements;

a preformed dielectric element having a plurality of cavities formed therethrough disposed between the first semiconductor component substrate and the second semiconductor component substrate with an interconnect element of each of the first and second semiconductor component substrates aligned therewith to define a plurality of interconnect voids therebetween; and

a mass of conductive material within each cavity of the plurality in contact with an interconnect element of each of the first and second semiconductor component substrates.

53. The assembly according to claim 52, wherein the mass of conductive material within each cavity of the plurality substantially fills that cavity.

54. The assembly according to claim 52, further including an aperture extending from each interconnect void of the plurality to an exposed surface of the first or second semiconductor component substrates.

55. The assembly according to claim 54, wherein the aperture is occluded with a dielectric sealing material.

56. The assembly according to claim 52, wherein the first semiconductor component substrate having a plurality of interconnect elements on a surface thereof comprises a semiconductor die having a plurality of bond pads on a surface thereof.

57. The assembly according to claim 52, wherein the second semiconductor component substrate having another like plurality of interconnect elements on a surface thereof comprises a carrier substrate having a plurality of terminal pads on a surface thereof.

58. The assembly according to claim 52, wherein the mass of conductive material comprises one of a conductive polymer, a conductor-filled polymer and a solder.

59. The assembly according to claim 52, wherein one of the first and second semiconductor component substrates comprises a semiconductor die and another of the first and second semiconductor component substrates comprises a carrier substrate.